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ATTORNEY'S DOCKET NUMBER
107280

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

U.S. APPLICATION NO. (if known, see 37 C.F.R. 1.5)
09/673479

414 Rec'd PCT/PTO 16 OCT 2000

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/JP00/00710	February 9, 2000	February 18, 1999

TITLE OF INVENTION
BINDER, SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME, CIRCUIT BOARD, AND ELECTRONIC EQUIPMENT

APPLICANT(S) FOR DO/EO/US
Nobuaki HASHIMOTO

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.

2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.

3. ☒ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).

4. ☐ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.

5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)

6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).

7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☒ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.

8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).

9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).

10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 11. to 16. below concern other document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.

12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.

13. ☒ A FIRST preliminary amendment.

    ☐ A SECOND or SUBSEQUENT preliminary amendment.

14. ☐ A substitute specification.

15. ☐ Entitlement to small entity status is hereby asserted.

16. ☐ Other items or information:

U.S. APPLICATION NO. (if known, see 37 C.F.R. 1.5) 09/673479	INTERNATIONAL APPLICATION NO. PCT/JP00/00710	ATTORNEY'S DOCKET NUMBER 107280

17. ☒ The following fees are submitted:	CALCULATIONS	PTO USE ONLY
Basic National fee (37 CFR 1.492(a)(1)-(5)):		
Search Report has been prepared by the EPO or JPO $860.00		
International preliminary examination fee paid to USPTO (37 CFR1.482) $690.00		
No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)) $710.00		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO.....$1,000.00		
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4).....$ 100.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$860	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$	

Claims	Number Filed	Number Extra	Rate		
Total Claims	28 - 20 =	8	X $ 18.00	$144	
Independent Claims	4 - 3 =	1	X $ 80.00	$80	
Multiple dependent claim(s)(if applicable)			+ $270.00	$	
TOTAL OF ABOVE CALCULATIONS =				$1,084	
Reduction by 1/2 for filing by small entity, if applicable.			-	$	
SUBTOTAL =				$1,084	
Processing fee of $130.00 for furnishing the English translation later than ☐ 20 ☐ 30 month from the earliest claimed priority date (37 CFR 1.492(f)).			+	$	
TOTAL NATIONAL FEE =				$1,084	
				Amount to be refunded	$
				Charged	$

a. ☒ Check No. 112822 in the amount of $1,084 to cover the above fees is enclosed.
b. ☐ Please charge my Deposit Account No. _____ in the amount of $_____ to cover the above fees. A duplicate copy of this sheet is enclosed.
c. ☒ The Director is hereby authorized to charge any additional fees which may be required, or credit any overpayment, to Deposit Account No. 15-0461. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Nobuaki HASHIMOTO

Application No.: U.S. National Stage PCT/JP00/00710

Filed: October 16, 2000 Docket No.: 107280

For: BINDER, SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME, CIRCUIT BOARD, AND ELECTRONIC EQUIPMENT

PRELIMINARY AMENDMENT

Director of the U.S. Patent and Trademark Office
Washington, D. C. 20231

Sir:

Prior to initial examination and after entry of the Article 19 Amendments, please amend the above-identified application as follows:

IN THE SPECIFICATION:

Pager 17, line 10, change "32" to --34--.

line 11, change "34" to --32--.

IN THE CLAIMS:

Please amend claims 13, 18-20, and 27-28 as follows:

Claim 13, line 4, change "first" to --second--.

line 5, change "second" to --first--.

Claim 18, lines 2 and 3, change "any one of Claims 4 to 14" to --Claim 4--.

Claim 19, line 2, change "any one of Claims 15 to 17" to --Claim 15--.

Claim 20, line 2, change "any one of Claims 15 to 17" to --Claim 15--.

Claim 27, line 2, change "any one of Claims 21 to 24" to --Claim 21--.

Claim 28, line 2, change "Claims 25 or 26" to --Claim 25--.

REMARKS

Claims 1-28 are pending. By this Preliminary Amendment, the specification and claims 13 are amended to eliminate typographical errors, and claims 18-20 and 27-28 are amended to eliminate multiple dependencies. Prompt and favorable examination on the merits is respectfully solicited.

Respectfully submitted,

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BINDER, SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME, CIRCUIT BOARD, AND ELECTRONIC EQUIPMENT

Technical Field

The present invention relates to a binder, a semiconductor device as well as a method of manufacturing the same, a circuit board, and electronic equipment.

Background of Art

A semiconductor chip and a substrate often differ much in the coefficients of thermal expansion, and particularly when they are cooled after heating, a stress incurred by the difference of the coefficients of thermal expansion is exerted on a binder. Herein, there has been the possibility that the separation of the binder will arise.

Further, in case of employing an anisotropic conductive binder as the binder by way of example, it has sometimes been difficult that an insulating resin is caused to flow out with conductive particles left behind between the bump of the semiconductor chip and a interconnecting pattern formed in the substrate, when the anisotropic conductive film is pressed by the semiconductor chip and the substrate.

These problems are ascribable to the fact that different properties are required for both the surfaces of the binder, and binders in the related art have failed to cope with the requirement.

The present invention consists in solving the problems as

stated above, and has for its object to provide a binder which can cope with the requirement of the different properties for both the surfaces thereof, and a semiconductor device as well as a manufacturing method therefor, a circuit board, and electronic equipment which use the binder.

Disclosure of Invention

(1) A binder according to the present invention is used for bonding electronic components, a physical property of the binder is different in a thickness direction thereof.

Since the physical property differs on both the surfaces of the binder, the binder can be constructed so as to be suited to materials which are to be bonded to the respective surfaces.

(2) The binder may be an anisotropic conductive film.

Even the anisotropic conductive film can be constructed so as to be suited to materials which are to be bonded to the respective surfaces.

(3) The binder may form a two-layer structure comprising a first layer formed of a first resin as a base material and a second layer formed of a second resin as a base material, and the first resin and the second resin may have different physical properties.

According to this, the first resin constituting the first layer, and the second resin constituting the second layer have the different physical properties. Thus, the first resin and the second resin can be selected so as to have physical properties respectively suited to a member which adheres to the

first layer, and a member which adheres to the second layer.

(4) In this binder,

a coefficient of thermal expansion of the first resin may be smaller than a coefficient of thermal expansion of the second resin.

When the first layer adheres to the member having the small coefficient of thermal expansion, and the second layer adheres to the member having the large coefficient of thermal expansion, the first and second resins have the coefficients of thermal expansion corresponding to the respective members, and hence, separation hardly occurs.

(5) In this binder,

the silica-based filler may be mixed only in the first resin.

Thus, the coefficient of thermal expansion of the first resin can be made small, and more specifically, it can be brought close to the coefficient of thermal expansion of silicon.

(6) In this binder,

the silica-based filler may be mixed in the first resin and the second resin, and a mixing ratio of the silica-based filler in the first resin may be greater than a mixing ratio of the silica-based filler in the second resin.

Thus, the coefficient of thermal expansion of the first resin can be made smaller than the coefficient of thermal expansion of the second resin, and more specifically, it can be brought close to the coefficient of thermal expansion of silicon.

(7) In this binder,

the second resin may be made lower in elasticity than the first resin.

Thus, when the second layer adheres to the member having the large coefficient of thermal expansion, the second resin is easy of elongation and has a high flexibility, and hence, separation hardly occurs.

(8) In this binder,

the second resin may be a metamorphic epoxy resin.

Thus, the second resin can be made low in elasticity.

(9) In this binder,

the first resin may be an epoxy resin, and

the second resin may be a biphenyl resin.

Thus, the second resin becomes lower in elasticity than the first resin.

(10) In this binder,

conductive particles may be dispersed only in the second resin.

Thus, the conductive particles do not touch the surface of the member adhering to the first layer, and hence, electrical short-circuiting does not occur.

(11) In this binder,

the conductive particles may be dispersed only in the second resin; and

the second layer may be thinner than the first layer, and the second resin may have higher viscosity than the first resin when melted.

According to this, since the conductive particles are dispersed only in the second resin, they do not touch the surface of the member adhering to the first layer, and hence, electrical short-circuiting does not occur. In addition, since the second layer is thinner than the first layer, the electrical short-circuiting can be prevented with the number of the conductive particles decreased. Further, although that the conductive particles are small in number, they can be reliably left behind because of the high melt viscosity of the second resin. Meantime, the first resin lower in the melt viscosity than the second resin is easy to outflow.

(12) In this binder,

the silica-based filler may be mixed only in the second resin.

Thus, the melt viscosity of the second resin can be made higher.

(13) In this binder,

the silica-based filler may be mixed in the first resin and the second resin, and a mixing ratio of the silica-based filler in the first resin may be greater than a mixing ratio of the silica-based filler in the second resin.

Thus, the melt viscosity of the second resin can be made higher.

(14) In this binder,

a molecular weight of the second resin may be greater than a molecular weight of the first resin.

Thus, the melt viscosity of the second resin can be made

higher.

(15) A semiconductor device according to the present invention comprises:

a semiconductor chip;

a substrate on which a interconnecting pattern is formed; and

a binder electrically connecting the semiconductor chip and the interconnecting pattern,

wherein a physical property of the binder being different in a thickness direction thereof.

Since the physical property differs on both the surfaces of the binder, the binder can be constructed so as to be suited to materials which are to be bonded to the respective surfaces.

(16) In this semiconductor device,

the binder may be an anisotropic conductive film.

Even the anisotropic conductive film can be constructed so as to be suited to materials which are to be bonded to the respective surfaces.

(17) In this semiconductor device,

the binder may form a two-layer structure comprising a first layer formed of a first resin as a base material and disposed on a side of the semiconductor chip, and a second layer formed of a second resin as a base material and disposed on a side of the substrate, and the first resin and the second resin may have different physical properties.

According to this, the first resin constituting the first layer of the binder, and the second resin constituting the

second layer have the different physical properties. Accordingly, the first resin and the second resin can be selected so as to have physical properties respectively suited to the semiconductor chip which adheres to the first layer, and the substrate which adheres to the second layer.

(18) In this semiconductor device,

the binder may be the binder as mentioned above.

(19) On a circuit board according to the present invention, the semiconductor device as mentioned above is mounted.

(20) Electronic equipment according to the present invention comprises the semiconductor device as mentioned above.

(21) A method of manufacturing a semiconductor device according to the present invention comprises a step of providing a binder between a semiconductor chip and a interconnecting pattern of a substrate on which is formed the interconnecting pattern, pressing the semiconductor chip and the substrate, and electrically connecting the semiconductor chip and the interconnecting pattern,

wherein the binder differs in a physical property in a thickness direction thereof.

Since the physical property differs on both the surfaces of the binder, the binder can be constructed so as to be suited to materials which are to be bonded to the respective surfaces.

(22) In this method of manufacturing a semiconductor device,

the binder may be an anisotropic conductive film.

Even the anisotropic conductive film can be constructed so as to be suited to materials which are to be bonded to the respective surfaces.

(23) In this method of manufacturing a semiconductor device,

the binder may form a two-layer structure comprising a first layer formed of a first resin as a base material, and a second layer formed of a second resin as a base material, and the first resin and the second resin may have different physical properties.

According to this, the first resin constituting the first layer of the binder, and the second resin constituting the second layer have the different physical properties. Accordingly, the first resin and the second resin can be selected so as to have physical properties suited for adhesion for the semiconductor chip and the substrate.

(24) In this method of manufacturing a semiconductor device,

the second layer may be formed after the first layer.

(25) In this method of manufacturing a semiconductor device,

the first layer may be disposed on a side of the semiconductor chip, and the second layer may be disposed on a side of the substrate.

According to this, the first resin and the second resin can be selected so as to have physical properties respectively suited to the semiconductor chip which adheres to the first

layer, and the substrate which adheres to the second layer.

(26) In this method of manufacturing a semiconductor device,

the binder may be the binder mentioned above.

Brief Description of Drawings

Fig. 1A to Fig. 1C are views showing a method of manufacturing a semiconductor device according to an embodiment of the present invention.

Fig. 2 is a view showing a circuit board according to an embodiment of the present invention.

Fig. 3 is a view showing electronic equipment which includes the semiconductor device manufactured by applying the method according to the present invention.

Best Modes for Carrying Out the Invention

Now, preferred embodiments of the present invention will be described with reference to the drawings.

Fig. 1A to Fig. 1C are views showing a method of manufacturing a semiconductor device according to an embodiment the present invention. Shown in Fig. 1C is the semiconductor device 1 finished up by the manufacturing method.

The semiconductor device 1 includes a semiconductor chip 10 and a substrate 20. In a case where the planar shape of the semiconductor chip 10 is a rectangle (a regular square or an oblong), a plurality of electrodes 12 are formed on one surface (active surface) of the semiconductor chip 10 along "at least

one edge" (comprehending "two opposing edges" or "all edges"). Alternatively, a plurality of electrodes 12 may well be formed on the central part of one surface of the semiconductor chip 10. The electrodes 12 are often provided with bumps 14 by solder balls, gold wire balls, gold plating or the like, but this is not indispensable. The electrodes 12 themselves may well be in the shape of bumps. Nickel, chromium, titanium or the like may well be added between the electrodes 12 and the bumps 14 as a layer preventive of the diffusion of a bump metal.

The shape of the whole substrate 20 may be any of a rectangle, a polygon, or a shape with a plurality of rectangles combined, without being especially restricted, and it can be made similar to the planar shape of the semiconductor chip 10. Although the thickness of the substrate 20 is often determined by the quality of the material thereof, it is not restricted, either. The substrate 20 may be formed of any of organic type and inorganic type materials and may well be made of a composite structure of these materials, but preferably it can be punched through. The substrate 20 can be formed by punching through a tape-like flexible substrate which is formed of an organic type material.

A multilayer substrate or a build-up type substrate may well be employed as the substrate 20. In case of utilizing the build-up type substrate or the multilayer substrate, when a interconnecting pattern is formed on a ground layer spreading planarly, a microstrip structure having no surplus interconnecting pattern is obtained, and hence, the transmission characteristics of signals can be enhanced.

A plurality of interconnections (leads) are formed on one surface of the substrate 20, thereby to construct the interconnecting pattern 22. At least one or all of the plurality of interconnections is/are not in electrical conduction with any other interconnection, and is/are electrically independent. Alternatively, those of a plurality of interconnections which are connected to the common locations, such as power supply and ground, of the semiconductor chip 10 may well be interconnected. Land portions are formed at both the ends of each interconnection. Each of the land portions is often formed so as to have a width greater than that of the portion which connects between both the land portions. It is also allowed to form one of the land portions at that position of the substrate 20 which is near the end part of the semiconductor device being the final product, and to form the other land portion at that position of the substrate 20 which is near the central part thereof. Bumps may well be formed at those parts (for example, the land portions) of the interconnecting pattern 22 which are bonded with the electrodes 12 of the semiconductor chip 10. In that case, the bumps 14 of the semiconductor chip 10 can also be omitted.

A plurality of through holes 24 are formed in the substrate 20. The interconnecting pattern 22 is so formed that any of the interconnections passes on each of the through holes 24. The end part of the interconnection may well overlie the through hole 24. In a case where the land portion is formed at the end part of the interconnection, it overlies the through hole 24.

As shown in Fig. 1C, the substrate 20 is provided with external terminals 40. Solder balls may well be used as the external terminals 40. The external terminals 40 are electrically connected to the interconnecting pattern 22. The external terminals 40 can be electrically connected to the interconnecting pattern 22 by, for example, providing conductive members in the through holes 24 by plating or the like, or disposing a solder in the through holes.

Plating is performed for the interconnecting pattern 22. The interconnecting pattern 22 can be formed of copper, and plated with nickel, gold, a solder or tin. A conductivity is ensured by performing the plating. Concretely, good soldering with the external terminal 40 is permitted, the oxidation of the surfaces of the interconnection is prevented, and the resistance of electrical connection with the bump is lowered.

The semiconductor chip 10 is mounted on the substrate 20 in face-down fashion. The bumps 14 of the semiconductor chip 10 and the interconnecting pattern 22 formed on the substrate 20 are electrically connected. In the present invention, the external terminals 40 stated above are not always necessary. Required, at least, is a construction which has the semiconductor chip 10 and the substrate 20 formed with the opposing interconnecting pattern 22, and in which a binder 30 exists between the semiconductor chip 10 and the substrate 20. The binder 30 may be, at least, of a resin (an underfill resin) having an insulating property, and it may well be of a resin having an anisotropic conductivity. Regarding the face-down

bonding between the bumps 14 of the semiconductor chip 10 and the interconnecting pattern 22 of the substrate 20, there have been known a method which is based on intermetallic bonding with a brazing material such as solder, or the like, a method which holds a mechanical bonding strength by utilizing the shrinkage of a resin, a method which heats and presses the semiconductor chip bearing the gold bumps (if necessary, ultrasonic bonding is performed), a method which employs an anisotropic conductive film, and so forth, and any of the methods may be applied.

The binder 30 forms a two-layer structure which comprise a first layer 32 and a second layer 34. The first layer 32 is made of a first resin, while the second layer 34 is made of a second resin. In this embodiment, the first resin and the second resin have different physical properties. Shown in Fig. 1A is an example in which the anisotropic conductive film is used as the binder 30. The binder 30 is such that conductive particles 36 are dispersed in a binder.

(The case where the coefficients of thermal expansion are different)

The coefficient of thermal expansion of the first resin (for example, 20 to 40 (10^{-6}/°C)) may well be smaller than the coefficient of thermal expansion of the second resin (for example, 40 to 200 (10^{-6}/°C)). The first layer 32 made of the first resin adheres to the semiconductor chip 10, while the second layer 34 made of the second resin adheres to the substrate 20. Here, the semiconductor chip 10 is often made of a material

of which coefficient of thermal expansion is small (for example, silicon), while the substrate 20 is often made of a material of which coefficient of thermal expansion is large (for example, a polyimide resin).

The difference of the coefficients of thermal expansion is small between the first layer 32 made of the first resin having the small coefficient of thermal expansion and the semiconductor chip 10 having the small coefficient of thermal expansion, so that the separation of the binder 30 is difficult to occur. In order to bring the coefficient of thermal expansion of the first resin close to the coefficient of thermal expansion of silicon, a silica-based filler may well be mixed in the first resin at a mixing ratio of, for example, 30% to 60%. In that case, the silica-based filler should preferably be prevented from mixing in the second resin. Alternatively, even when the silica-based filler is mixed in the first resin and the second resin, the mixing ratio of the silica-based filler in the first resin may be greater than that of the same in the second resin. In that case, the difference of the mixing ratios of the silica-based filler should preferably be on the order of 30% to 60%.

The difference of the coefficients of thermal expansion is small between the second layer 34 made of the second resin having the large coefficient of thermal expansion and the substrate 20 having the large coefficient of thermal expansion, so that the separation of the binder 30 is difficult to occur.

In the case where the anisotropic conductive film is

employed as the binder 30, and where the coefficients of thermal expansion of the first and second resins are different, the conductive particles 36 may well be dispersed in only one of the resins. Concretely, the conductive particles 36 should preferably be dispersed only in the second layer 34 which adheres to the interconnecting pattern 22 having an electrical connection area larger than that of the bumps 14 of the semiconductor chip 10. Thus, when the bumps 14 have sunk in the binder 30 (anisotropic conductive film), the probability at which the conductive particles 36 remain under the bumps 14 heightens to enhance the reliability of electrical connections. Moreover, since the conductive particles 36 are not dispersed in the first layer 32 adhering to the semiconductor chip 10, the short-circuiting between the electrodes 12 of the semiconductor chip 10 is prevented.

(The case where the elastic moduli are different)

The second resin may well be made lower in elasticity than the first resin. By way of example, it is also allowed that the elastic modulus of the first resin is about 3 to 10 (GPa), while the elastic modulus of the second resin is about 1 GPa to 3 GPa. Thus, when the second layer 34 made of the second resin adheres to the substrate 20 having the large coefficient of thermal expansion, the second resin is easy of elongation and has a high conformability, so that the separation becomes difficult to occur.

In order to lower the elasticity of the second resin, an

epoxy resin may well be metamorphosed as such. Alternatively, it is also allowed that the first resin is the epoxy resin, while the second resin is a biphenyl resin.

Also in the case where the anisotropic conductive film is employed as the binder 30, and where the elastic moduli of the first and second resins is different, the conductive particles 36 may well be dispersed in only one of the resins. Concretely, the conductive particles 36 should preferably be dispersed only in the second resin constituting the second layer 34 which adheres to the interconnecting pattern 22 having an electrical connection area larger than that of the bumps 14 of the semiconductor chip 10. Thus, when the bumps 14 have sunk in the binder 30, the probability at which the conductive particles 36 remain under the bumps 14 heightens to enhance the reliability of electrical connections. Moreover, since the conductive particles 36 are not dispersed in the first resin constituting the first layer 32 adhering to the semiconductor chip 10, the short-circuiting between the electrodes 12 of the semiconductor chip 10 is prevented.

(The case where melt viscosities are different)

In the case of employing the anisotropic conductive film as the binder 30, the second resin may well be higher than the first resin in the viscosity of a melted state. Thus, when the bumps 14 have sunk in the binder 30, the first resin of low melt viscosity is easy of outflow, and the second resin of high melt viscosity is difficult of outflow. Since the melt viscosity

of the second resin is high, the conductive particles 36 are easy to remain on the interconnecting pattern 22. In this case, the conductive particles 36 may well be dispersed in only the second resin constituting the second layer 34 which adheres to the interconnecting pattern 22. Since the conductive particles 36 are not dispersed in the first resin constituting the first layer 32 adhering to the semiconductor chip 10, the short-circuiting between the electrodes 12 of the semiconductor chip 10 is prevented.

Further, the second layer 32 may well be thinner than the first layer 34. Thus, the electrical short-circuiting can be prevented with the number of the conductive particles 36 decreased, and notwithstanding that the conductive particles 36 are small in number, they can be reliably left behind on the interconnecting pattern 22 owing to the high melt viscosity of the second resin.

In the case of employing the anisotropic conductive film as the binder 30, a silica-based filler may well be mixed in only the second resin in order to make the melt viscosity of the second resin higher than that of the first resin. Alternatively, it is also allowed to mix the silica-based filler in the first resin and second resin, and to make the mixing ratio of the silica-based filler in the second resin greater than that of the same in the first resin. Alternatively, it is also allowed to set the molecular weight of the second resin larger than that of the first resin.

While, in the above, the two layers of resins having the

different physical properties have been stated as to this embodiment, the difference of the physical properties between the layers should more preferably change continuously, not stepwise, and this is more meritorious because the difference of the physical properties in the thickness direction of the layers is not existent. The reason is that the separation, etc. ascribable to the difference of the physical properties at the interface of the two layers are difficult to arise. Concretely, multilayer resins of which physical properties are different with small differences, or resins of which physical properties change continuously in the thickness direction thereof can be used for that purpose.

Two layers of anisotropic conductive films are obtained in such a way that a single layer of anisotropic conductive film is prepared in the shape of a sheet, whereupon a single layer of anisotropic conductive film having a different physical property is further prepared on the first-mentioned layer in the shape of a sheet. The subsequent handling is the same as in the single layer of anisotropic conductive film. In case of more layers of anisotropic conductive films, these operations are repeated. In forming an anisotropic conductive film of which physical property differs continuously in the thickness direction thereof, the interdiffusion between layers is induced by solvents which are used when the two or more layers of anisotropic conductive films are prepared, or by some heating. Thus, the continuous layer can be obtained.

The semiconductor device according to this embodiment is

constructed as stated above, and a method of manufacturing it will be described below.

As shown in Fig. 1A, the surface of a semiconductor chip 10 formed with electrodes 12 (or bumps 14) and the surface of a substrate 20 formed with a interconnecting pattern 22 are disposed so as to oppose to each other. In addition, a binder 30 is disposed between the semiconductor chip 10 and the substrate 20. More specifically, the binder 30 is interposed with its first layer 32 confronted to the semiconductor chip 10 and its second layer 34 confronted to the substrate 20. Incidentally, the binder 30 should preferably be stuck onto either of the semiconductor chip 10 and the substrate 20 beforehand.

In a case where the binder 30 formed of a plurality of layers (for example, the two layers of first and second layers 32, 34), the respective layers of the plurality of layers (for example, the first layer 32 and the second layer 34) may well be disposed in succession. More specifically, it is also allowed to successively dispose the layers by attaching the corresponding layer to either the semiconductor chip 10 or the substrate 20, or to attach either layer (for example, the first layer 32) to the semiconductor chip 10, followed by attaching the other layer (for example, the second layer 34) to the substrate 20.

As shown in Fig. 1B, the semiconductor chip 10 and the substrate 20 are brought into adhesion through the binder 30. More specifically, the semiconductor chip 10 and the substrate 20 are pressed in the direction of narrowing the spacing between

the two. Thus, conductive particles 36 are interposed between the electrodes 12 (or bumps 14) of the semiconductor chip 10 and the interconnecting pattern 22, whereby the electrical connections between the two are established.

As shown in Fig. 1C, external terminals 40 are provided on the substrate 20, whereby the semiconductor device 1 can be obtained. Although the semiconductor device of FAN-IN type in which the external terminals 40 are disposed only within the mounting area of the semiconductor chip 10 is shown in Fig. 1C, the present invention is not restricted thereto. The present invention is also applicable to, for example, a semiconductor device of FAN-OUT type in which external terminals 40 are disposed only outside the mounting area of the semiconductor chip 10, and a semiconductor device of FAN-IN/OUT type in which the FAN-OUT type is combined with the FAN-IN type. By the way, in the semiconductor device of the FAN-OUT type or the FAN-IN/OUT type, a stiffener may well be stuck outside the semiconductor chip by employing an anisotropic conductive film.

In this embodiment, the binder 30 comprising the first and second layers 32, 34 is used, so that the effects stated above can be accomplished.

Although this embodiment has been described concerning the example in which the semiconductor chip 10 is mounted on the substrate 20 of BGA (Ball Grid Array) type in face-down fashion, it is as stated before that, without regard to the structural aspect of the substrate 20, the invention can be applied to any mounting aspect in which the semiconductor chip 10 is merely

subjected to the face-down mounting on the substrate 20.

Shown in Fig. 2 is a circuit substrate 50 in which the semiconductor device 1 according to this embodiment is mounted. It is common to employ an organic type substrate, for example, a glass epoxy substrate, as the circuit board 50. A interconnecting pattern 52 made of, for example, copper is formed in the circuit board 50 so as to become a desired circuit, and the interconnecting pattern and the external terminals 40 of the semiconductor device 1 are mechanically connected, thereby to attain the electrical conduction thereof.

Besides, a notebook type personal computer is shown in Fig. 3 as electronic equipment 60 having the semiconductor device 1 to which the present invention is applied.

Incidentally, an electronic component can also be manufactured by substituting an "electronic element" for the constituent requisite "semiconductor chip" of the present invention and mounting the electronic element (irrespective of whether it is an active element or a passive element) on a substrate likewise to the semiconductor chip. The electronic component which is manufactured using such an electronic element is, for example, a resistor, a capacitor, a coil, an oscillator, a filter, a temperature sensor, a thermistor, a varistor, a volume controller or a fuse.

CLAIMS

1. (Amended) A binder used for bonding electronic components, a physical property of the binder being different in a thickness direction thereof in a state where the binder is bonded with at least the electronic components.

2. The binder as defined in Claim 1,

wherein the binder is an anisotropic conductive film.

3. (Amended) The binder as defined in Claim 2,

wherein the binder forms a two-layer structure comprising a first layer formed of a first resin as a base material, and a second layer formed of a second resin as a base material, the first resin and the second resin having different physical properties in a state where the binder is bonded with at least the electronic components..

4. The binder as defined in Claim 3,

wherein a coefficient of thermal expansion of the first resin is smaller than a coefficient of thermal expansion of the second resin.

5. The binder as defined in Claim 4,

wherein the silica-based filler is mixed only in the first resin.

6. The binder as defined in Claim 4,

wherein the silica-based filler is mixed in the first resin and the second resin, and a mixing ratio of the silica-based filler in the first resin is greater than a mixing ratio of the silica-based filler in the second resin.

7. (Amended) The binder as defined in Claim 3,

wherein the second resin is made lower in elastic modulus than the first resin.

8. The binder as defined in Claim 7,

wherein the second resin is a metamorphic epoxy resin.

9. The binder as defined in Claim 7,

wherein the first resin is an epoxy resin, and

wherein the second resin is a biphenyl resin.

10. The binder as defined in Claim 3,

wherein conductive particles are dispersed only in the second resin.

11. The binder as defined in Claim 3,

wherein the conductive particles are dispersed only in the second resin; and

wherein the second layer is thinner than the first layer, and the second resin has higher viscosity than the first resin when melted.

12. The binder as defined in Claim 11,

wherein the silica-based filler is mixed only in the second resin.

13. The binder as defined in Claim 11,

wherein the silica-based filler is mixed in the first resin and the second resin, and a mixing ratio of the silica-based filler in the first resin is greater than a mixing ratio of the silica-based filler in the second resin.

14. The binder as defined in Claim 11,

wherein a molecular weight of the second resin is greater than a molecular weight of the first resin.

15. (Amended) A semiconductor device comprising:

a semiconductor chip;

a substrate on which a interconnecting pattern is formed; and

a binder electrically connecting the semiconductor chip and the interconnecting pattern,

wherein the binder differs in a coefficient of thermal expansion or an elastic modulus in a thickness direction thereof.

16. The semiconductor device as defined in Claim 15,

wherein the binder is an anisotropic conductive film.

17. The semiconductor device as defined in Claim 16, wherein the binder forms a two-layer structure comprising a first layer formed of a first resin as a base material and disposed on a side of the semiconductor chip, and a second layer formed of a second resin as a base material and disposed on a side of the substrate, the first resin and the second resin having different physical properties.

18. The semiconductor device as defined in Claim 17, wherein the binder is the binder as defined in any one of Claims 4 to 14.

19. A circuit board on which the semiconductor device as defined in any one of Claims 15 to 17 is mounted.

20. Electronic equipment comprising the semiconductor device as defined in any one of Claims 15 to 17.

21. (Amended) A method of manufacturing a semiconductor device, comprising a step of providing a binder having a multilayer structure, between a semiconductor chip and a interconnecting pattern of a substrate on which is formed the interconnecting pattern, pressing the semiconductor chip and the substrate, and electrically connecting the semiconductor chip and the interconnecting pattern,

wherein a physical property of each layer of the binder having the multilayer structure is different from one another.

22. The method of manufacturing a semiconductor device as defined in Claim 21,

wherein the binder is an anisotropic conductive film.

23. (Amended) The method of manufacturing a semiconductor device as defined in Claim 22,

wherein the binder forms a two-layer structure comprising a first layer formed of a first resin as a base material, and a second layer formed of a second resin having a different coefficient of thermal expansion or an elastic modulus from the first resin as a base material.

24. The method of manufacturing a semiconductor device as defined in Claim 23,

wherein the second layer is formed after the first layer.

25. (Amended) A method of manufacturing a semiconductor device, comprising a step of providing a binder between a semiconductor chip and a interconnecting pattern of a substrate on which is formed the interconnecting pattern, pressing the semiconductor chip and the substrate, and electrically connecting the semiconductor chip and the interconnecting pattern,

wherein the binder comprises a first layer formed of a

first resin as a base material, and a second layer formed of a second resin as a base material, the second resin differing from the first resin in at least one of a coefficient of thermal expansion and an elastic modulus of, and

wherein the first layer is disposed on a side of the semiconductor chip, and the second layer is disposed on a side of the substrate.

26. (Amended) The method of manufacturing a semiconductor device as defined in Claim 25,

wherein at least one of the first layer and the second layer is an anisotropic conductive film.

27. (Amended) The method of manufacturing a semiconductor device as defined in any one of Claims 21 to 24,

wherein the binder is the binder as defined in any one of Claims 4 to 14.

28. (Amended) The method of manufacturing a semiconductor device as defined in Claims 25 or 26,

wherein the binder is the binder as defined in any one of Claims 4 to 14.

ABSTRACT

A semiconductor device (1) comprises a semiconductor chip (10), a substrate (20) which is formed with a interconnecting pattern (22), and a binder (30) which electrically connects the semiconductor chip (10) and the interconnecting pattern (22); the binder (30) forms a two-layer structure comprising a first layer (32) of which base material is a first resin and which is disposed on the side of the semiconductor chip (10), and a second layer (34) of which base material is a second resin and which is disposed on the side of the substrate (20); and the first resin and the second resin have different physical properties in the coefficients of thermal expansion, or the likes.

FIG. 1A

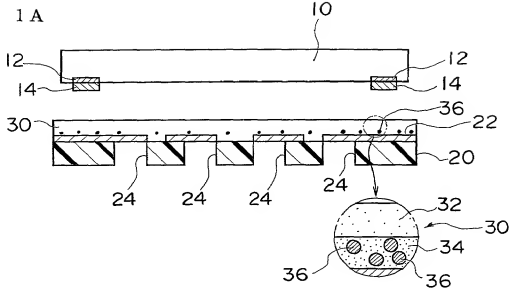


FIG. 1B

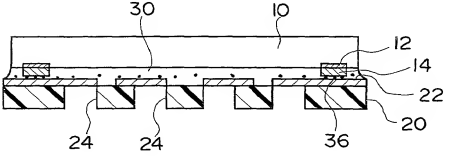


FIG. 1C

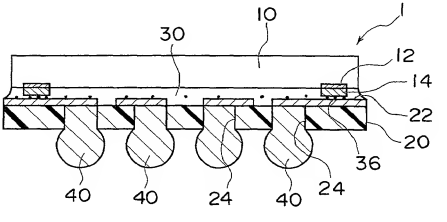


FIG. 2

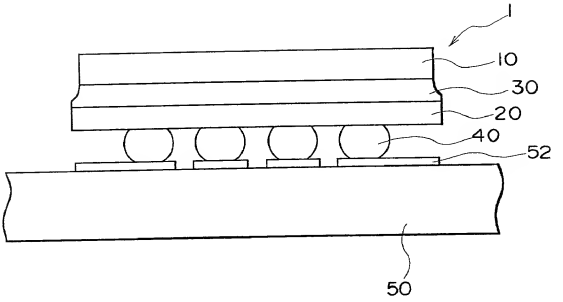
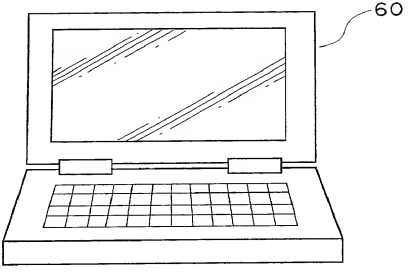


FIG. 3



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Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

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下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は、下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

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I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

接着部材、半導体装置及びその製造方法、回路基板並びに電子機器

BINDER, SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME, CIRCUIT BOARD, AND ELECTRONIC EQUIPMENT

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

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特許協定条約 国際出願番号を _____ とし、
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☐ was filed on _____
as United States Application Number or
PCT International Application Number
_____ and was amended on
_____ (if applicable).

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I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

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I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s) 外国での先行出願			Priority Not Claimed 優先権主張なし
11-039625(P) (Number) (番号)	JAPAN (Country) (国名)	18/February/1999 (Day/Month/Year Filed) (出願年月日)	☐
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	☐

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(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

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PCT/JP00/00710 (Application No.) (出願番号)	9/February/2000 (Filing Date) (出願日)	Pending (Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)
(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Kirk M. Hudson, (Reg. 27,562)
Thomas J. Pardini, (Reg. 30,411)
Edward P. Walker, (Reg. 31,450)
Robert A. Miller, (Reg. 32,771)
Mario A. Costantino, (Reg. 33,565)
Caroline D. Dennison, (Reg.34,494)

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